CLAIMS

What is claimed as new and desired to be protected by Letters Patent of the United States is:

1. A circuit, comprising:

first and a second input connections;

an amplifier having a first amplifier input, a second amplifier input, a first amplifier output, and a second amplifier output;

a first network that is switchable to receive at least a first differential input signal from said first and second input connections and a first differential feedback signal from said first and second amplifier outputs, and that provides said at least a first differential signal to the first and second inputs of said amplifier; and

a second switchable network that receives at least a second differential input signal from said first and second input connections and a second differential feedback signal from said first and second amplifier outputs, and that provides said at least second differential signal to the first and second input of said amplifier;

wherein said first and second network are switched so that at any given time only one of said first and second switchable networks is coupled to said first and second input connections, said first and second amplifier inputs, and said first and second amplifier outputs.

2. The circuit of claim 1, wherein said first and second networks each comprise an input capacitor and a feedback capacitor.

3. The circuit of claim 1, wherein

said first network is switched to be coupled to said first and second input connections, said first and second amplifier outputs, and said first and second inputs of said amplifier when a first clock signal is high;

said first network is switched to be decoupled from said first and second input connections, said first and second amplifier outputs, and said first and second inputs of said amplifier when the first clock signal is low;

said second network is switched to be coupled to said first and second input connections, said first and second amplifier outputs, and said first and second inputs of said amplifier when a second clock signal is high; and

said second network is switched to be decoupled from said first and second input connections, said first and second amplifier outputs, and said first and second inputs of said amplifier when the second clock signal is low.

4. The circuit of claim 3, wherein said first and second clock signals share a same period and are out of phase by half a period.

5. The circuit of claim 4, further comprising,

a clock generator;

wherein said clock generator accepts a master clock signal and produces the first clock signal and the second clock signal as alternating, non-overlapping signals.

6. The circuit of claim 3, wherein said first clock signal and said second clock signal each have a period equal that of said master clock signal.

7. The circuit of claim 6, wherein said first and second clock signals are out of phase by half a period.

8. A processor based system, comprising:

a processor; and

a circuit, coupled to said processor, said circuit further comprising,

a first and a second input connections;

an amplifier having a first amplifier input, a second amplifier input, a first amplifier output, and a second amplifier output;

a first network that is switchable to receive at least a first differential input signal from said first and second input connections and a first differential feedback signal from said first and second amplifier outputs, and that provides said at least a first differential signal to the first and second inputs of said amplifier; and

a second switchable network that receives at least a second differential input signal from said first and second input connections and a second differential feedback signal from said first and second amplifier outputs, and that provides said at least second differential signal to the first and second input of said amplifier;

wherein said first and second network are switched so that at any given time only one of said first and second switchable networks is coupled to said first and second input connections, said first and second amplifier inputs, and said first and second amplifier outputs.

9. The circuit of claim 8, wherein said first and second networks each comprise an input capacitor and a feedback capacitor.

10. The circuit of claim 8, wherein

said first network is switched to be coupled to said first and second input connections, said first and second amplifier outputs, and said first and second inputs of said amplifier when a first clock signal is high;

said first network is switched to be decoupled from said first and second input connections, said first and second amplifier outputs, and said first and second inputs of said amplifier when the first clock signal is low;

said second network is switched to be coupled to said first and second input connections, said first and second amplifier outputs, and said first and second inputs of said amplifier when a second clock signal is high; and

said second network is switched to be decoupled from said first and second input connections, said first and second amplifier outputs, and said first and second inputs of said amplifier when the second clock signal is low.

11. The circuit of claim 10, wherein said first and second clock signals share a same period and are out of phase by half a period.

12. The circuit of claim 11, further comprising,

a clock generator;

wherein said clock generator accepts a master clock signal and produces the first clock signal and the second clock signal as alternating, non-overlapping signals.

13. The circuit of claim 10, wherein said first clock signal and said second clock signal each have a period equal that of said master clock signal.

14. The circuit of claim 13, wherein said first and second clock signals are out of phase by half a period.

15. A pipelined analog to digital converter, comprising:

a plurality of stages, each stage further comprising,

an input terminal;

an output terminal;

an amplifier, coupled to said output terminal;

a first processing section for performing a partial analog to digital conversion of a first signal and for providing a first residual signal to said amplifier; and

a second processing section for performing a partial analog to digital conversion of a second signal and for providing a second residual signal to said amplifier;

a first digital block, for receiving results of a partial analog to digital conversion from the first processing section of each stage, and for providing a full analog to digital conversion of a first input signal; and

a second digital block, for receiving results of a partial analog to digital conversion from the second processing section of each stage, and for providing a full analog to digital conversion of a second input signal;

wherein said plurality of stages are arranged in a cascade so that the output terminal of one stage is coupled to the input terminal of a subsequent stage.

16. The pipelined analog to digital converter of claim 15, further comprising:

a clock generator;

wherein said clock generator accepts a master clock signal and produces the first clock signal and the second clock signal as alternating, non-overlapping signals.

17. The pipelined analog to digital converter of claim 16, wherein said first clock signal and said second clock signal each have a period equal that of said master clock signal

18. The pipelined analog to digital converter of claim 17,

wherein in each stage,

said amplifier amplifies said first residual signal when said first clock signal is at a second state; and

said amplifier amplifies said second residual signal when said second clock is at a second stage.

19. An integrated circuit, comprising:

a substrate; and

a pipelined analog to digital converter in the substrate, the converter comprising:

a plurality of stages, each stage further comprising,

an input terminal;

an output terminal;

an amplifier, coupled to said output terminal;

a first processing section for performing a partial analog to digital conversion of a first signal and for providing a first residual signal to said amplifier; and

a second processing section for performing a partial analog to digital conversion of a second signal and for providing a second residual signal to said amplifier;

a first digital block, for receiving results of a partial analog to digital conversion from the first processing section of each stage, and for providing a full analog to digital conversion of a first input signal; and

a second digital block, for receiving results of a partial analog to digital conversion from the second processing section of each stage, and for providing a full analog to digital conversion of a second input signal;

wherein said plurality of stages are arranged in a cascade so that the output terminal of one stage is coupled to the input terminal of a subsequent stage.

20. A processor based system, comprising:

a processor; and

an analog to digital converter, coupled to said processor, said analog to digital converter comprising:

a plurality of stages, each stage further comprising,

an input terminal;

an output terminal;

an amplifier, coupled to said output terminal;

a first processing section for performing a partial analog to digital conversion of a first signal and for providing a first residual signal to said amplifier; and

a second processing section for performing a partial analog to digital conversion of a second signal and for providing a second residual signal to said amplifier;

a first digital block, for receiving results of a partial analog to digital conversion from the first processing section of each stage, and for providing a full analog to digital conversion of a first input signal; and

a second digital block, for receiving results of a partial analog to digital conversion from the second processing section of each stage, and for providing a full analog to digital conversion of a second input signal;

wherein said plurality of stages are arranged in a cascade so that the output terminal of one stage is coupled to the input terminal of a subsequent stage.

21. The system of claim 20, further comprising:

a clock generator that receives a master clock signal and produces a first clock signal and a second clock signal as alternating, non-overlapping signals;

wherein said first clock signal and said second clock signal each have a period equal that of said master clock signal.

22. The system of claim 21,

wherein in each stage,

said amplifier amplifies said first residual signal when said first clock signal is at a second state and

said amplifier amplifies said second residual signal when said second clock is at a second stage.

23. A method for operating a switched capacitor amplifier, comprising:

receiving a master clock signal;

generating a first clock signal from said master clock signal;

generating a second clock signal from said master clock signal;

when the first clock signal is in a first state,

receiving a first input in a first capacitor network;

while the first clock signal is in a second state,

coupling the first capacitor network to an amplifier; and

amplifying said first input to produce a first output using said amplifier and said first capacitor network;

when the second clock signal is in the first state,

receiving a second input in a second capacitor network;

while the second clock signal is in the second state,

coupling the second capacitor network to an amplifier; and

amplifying said second input to produce a second output using said amplifier and said second capacitor network;

wherein only one of said first and second clock signals is in the first state at any time.

24. The method of claim 23, further comprising:

when the first clock signal is in the second state,

decoupling said second capacitor network from said amplifier; and

when the second clock signal is in the second state,

decoupling said first capacitor network from said amplifier;

wherein when said second clock signal is in the first state said first clock signal is in the second state, and when said first clock signal is in the first state said second clock signal is in the second state.

25. A method for converting analog signals into digital signals, comprising:

receiving a master clock signal;

generating a first clock signal from said master clock signal;

generating a second clock signal from said master clock signal;

when the first clock signal is in a first state,

at each one of a plurality of stages,

receiving a first input signal at an input terminal;

when the first clock signal is in a second state,

at each one of a plurality of stages,

partially converting the first input signal into a first partial digital signal;

generating a first residual signal equal to the input signal minus a signal equal in magnitude to said first partial digital signal;

amplifying said first residual signal; and

outputting said amplified first residual signal as the first input signal to a next one of said plurality of stage; and

at a first digital block,

receiving said first partial digital signal; and

outputting a first full digital signal based on each one of said first partial digital signals;

when the second clock signal is in the first state,

at each one of the plurality of stages,

receiving a second input signal at an input terminal;

when the second clock signal is in the second state,

at each one of the plurality of stages,

partially converting the second input signal into a second partial digital signal;

generating a second residual signal equal to the input signal minus a signal equal in magnitude to said second partial digital signal;

amplifying said second residual signal; and

outputting said amplified second residual signal as the second input signal to the next one of said plurality of stages; and

at a second digital block,

receiving said second partial digital signal; and

outputting a second full digital signal based on each one of said second partial digital signals;

wherein only one of said first and second clock signals is in the first state at any time.

26. The method of claim 25, wherein when said second clock signal is in a first state said first clock signal is in the second state, and when said first clock signal is in the first state said second clock signal is in the second state.

27. An imager comprising:

an imaging sensor;

at least one analog-to-digital converter, coupled to said imaging sensor, wherein said analog-to-digital converter further comprises,

a circuit, comprising:

a first and a second input connections;

an amplifier having a first amplifier input, a second amplifier input, a first amplifier output, and a second amplifier output;

a first network that is switchable to receive at least a first differential input signal from said first and second input connections and a first differential feedback signal from said first and second amplifier outputs, and that provides said at least a first differential signal to the first and second inputs of said amplifier; and

a second switchable network that receives at least a second differential input signal from said first and second input connections and a second differential feedback signal from said first and second amplifier outputs, and that provides said at least second differential signal to the first and second input of said amplifier;

wherein said first and second network are switched so that at any given time only one of said first and second switchable networks is coupled to said first and second input connections, said first and second amplifier inputs, and said first and second amplifier outputs.

28. An imager comprising:

an integrated circuit, the integrated circuit comprising:

a substrate;

an imaging sensor on the substrate;

at least one analog-to-digital converter on the substrate, coupled to said imaging sensor, wherein said analog-to-digital converter further comprises,

a circuit, comprising:

a first and a second input connections;

an amplifier having a first amplifier input, a second amplifier input, a first amplifier output, and a second amplifier output;

a first network that is switchable to receive at least a first differential input signal from said first and second input connections and a first differential feedback signal from said first and second amplifier outputs, and that provides said at least a first differential signal to the first and second inputs of said amplifier; and

a second switchable network that receives at least a second differential input signal from said first and second input connections and a second differential feedback signal from said first and second amplifier outputs, and that provides said at least second differential signal to the first and second input of said amplifier;

wherein

said first and second network are switched so that at any given time only one of said first and second switchable networks is coupled to said first and second input connections, said first and second amplifier inputs, and said first and second amplifier outputs.

29. A switched capacitor amplifier, comprising:

an amplifier;

a first capacitor network, controllably coupled to said amplifier; and

a second capacitor network, controllably coupled to said amplifier;

wherein only one of said first and second capacitor networks is coupled to said amplifier at any given time.

30. A circuit comprising:

first and second input connections;

a first switchable network that receives input signals from the first input connection and provides output signals to a first input of an amplifier; and

a second switchable network that receives input signals from the second input connection and that provides output signal to a second input of the amplifier;

the first and second switchable networks each including first and second subnetworks, the switchable networks switching together between a first state in which each network's first subnetwork receives an input signal and each network's second subnetwork provides an output signal and a second state in which each network's second subnetwork receives an input signal and each network's first subnetwork provides an output signal.

31. A method of operating an amplifier comprising:

alternating between first and second phases, each phase receiving two respective input signals;

during each first phase, providing the two input signals received during the preceding second phase as a differential signal to the amplifier; and

during each second phase, providing the two input signals received during the preceding first phase as a differential signal to the amplifier.

32. A circuit comprising:

an amplifier with first and second differential inputs; and

a switching network that alternates between first and second phases,

the switching network respectively receiving first and second input signals during each phase; the switching network, during each first phase, providing first and second input signals received during the preceding second phase as a differential signal to the amplifier;

the switching network, during each second phase providing the first and second input signals received during the preceding first phase as a differential signal to the amplifier.